CLAIMS

1. A differential drive circuit for low voltage differential signals, comprising:

a switching circuit composed of MOS transistors, and configured to be inputted thereto with differential signals and to output current signals;

an output circuit including an NMOS transistor connected at its one end to a power supply potential on a high potential side and at its other end to one node in the switching circuit, and operating as a source follower; and a PMOS transistor connected at its one end to a power supply potential on a low potential side and at its other end to other node in the switching circuit and operating as a source follower; and

a reference potential generating circuit that supplies reference potentials to gates of the NMOS transistor and the PMOS transistor, respectively, wherein

the reference potential generating circuit includes potential variable means for changing a differential potential with an offset potential being kept constant.

2. The differential drive circuit for low voltage differential signals according to claim 1, wherein

the switching circuit includes: a first transistor and a second transistor connected at their one ends to a

source of the NMOS transistor, forming a node; and a third transistor and a fourth transistor connected at their one ends to a source of the PMOS transistor, forming a node,

a node at which the first transistor and the third transistor are connected at their other ends and a node at which the second transistor and the fourth transistor are connected at their other ends form output terminals of the output circuit, and

a node at which the first transistor and the fourth transistor are connected at their gates and a node at which the second transistor and the third transistor are connected at their gates form input terminals for the differential signals.

3. The differential drive circuit for low voltage differential signals according to claim 1, wherein the reference potential generating circuit includes:

a first resistor connected between the power supply potential on the high potential side and the gate of the NMOS transistor;

a second resistor connected between the gate of the NMOS transistor and the gate of the PMOS transistor; and

a third resistor connected between the gate of the PMOS transistor and the power supply potential on the low potential side.

4. The differential drive circuit for low voltage differential signals according to claim 3, wherein the first resistor and the third resistor in the reference potential generating circuit have an equal resistance value.

5. The differential drive circuit for low voltage differential signals according to claim 1, wherein

the reference potential generating circuit includes:

a first circuit group composed of a plurality of PMOS transistors connected in series and a plurality of resistors connected in series, which are connected in parallel;

a second circuit group composed of a plurality of NMOS transistors connected in series and a plurality of resistors connected in series, which are connected in parallel; and

a resistor connected between the resistors in the first circuit group and the resistors in the second circuit group, and wherein the resistors in the first circuit group and the resistors in the second group are set to an equal resistance value, the resistance value being changeable by controlling gates of the transistors in the first and the second circuit groups.

6. The differential drive circuit for low voltage differential signals according to claim 1, wherein the

reference potential generating circuit includes:

a first circuit group further including:

a first NMOS transistor connected at its drain to the power supply potential on the high potential side;

a second NMOS transistor connected at its drain to a source of the first NMOS transistor and at its gate to the power supply potential on the high potential side;

a third NMOS transistor connected at its source to the power supply potential on the low potential side;

a fourth NMOS transistor connected at its source to a drain of the third NMOS transistor and at its gate to the power supply potential on the high potential side;

a first resistor and a second resistor connected between a source of the second NMOS transistor and a drain of the fourth NMOS transistor;

a first differential amplifier having an output terminal connected to gates of the first NMOS transistor and a fifth NMOS transistor and controlling potentials of the gates, and operating such that a potential of a node at which the first resistor and the second resistor are connected approximates a first reference potential; and

the current source variable means that controls a current of the third NMOS transistor connected at its source to the power supply potential on the low potential side; and

a second circuit group further including:

the fifth NMOS transistor connected at its drain to the power supply potential on the high potential side;

a sixth NMOS transistor connected at its drain to a source of the fifth NMOS transistor and at its gate to the power supply potential on the high potential side, and a seventh PMOS transistor connected at its drain to the power supply potential on the low potential side;

an eighth NMOS transistor connected at its source to a source of the seventh PMOS transistor and at its gate to the power supply on the high potential side, and a third resistor and a fourth resistor connected between a source of the sixth NMOS transistor and a drain of the eighth NMOS transistor; and

a second differential amplifier having an output terminal connected to a gate of the seventh PMOS transistor and controlling a potential of the gate, and operating such that a potential of a node at which the third resistor and the fourth resistor are connected approximates the first reference potential.

7. The differential drive circuit for low voltage differential signals according to claim 6, wherein resistance values of the first resistor, the second resistor, the third resistor, and the fourth resistor in the reference potential generating circuit are n/2 (n is a positive integer value) times a resistance value of a

terminating resistor connected to output terminals of the output circuit.

8. The differential drive circuit for low voltage differential signals according to claim 6, wherein

a size of the first NMOS transistor and that of the fifth NMOS transistor in the reference potential generating circuit are 1/n (n is a positive integer value) of a size of the NMOS transistor, respectively, and

a size of the seventh PMOS transistor is 1/n (n is a positive integer value) of a size of the PMOS transistor.

9. The differential drive circuit for low voltage differential signals according to claim 1,

wherein output terminals of the output circuit are connected to output terminals of an emphasis circuit,

wherein the emphasis circuit includes a switching circuit for the emphasis circuit constituted by MOS transistors, which are inputted thereto with different differential signals, and output current signals, one node in the switching circuit for the emphasis circuit being connected to a drain of a PMOS transistor, a source of the PMOS transistor connected to the power supply potential on the high potential side, and a gate of the PMOS transistor connected to one terminal of a bias power supply for the emphasis circuit, and

wherein the other node in the switching circuit

for the emphasis circuit is connected to a drain of an NMOS transistor, a source of the NMOS transistor being connected to the power supply on the low potential side, and a gate of the NMOS transistor being connected to the other terminal of the bias power supply for the emphasis circuit.

10. The differential drive circuit for low voltage differential signals according to claim 9, wherein the switching circuit for the emphasis circuit is the switching circuit according to claim 2.

11. The differential drive circuit for low voltage differential signals according to claim 9, wherein the emphasis circuit is configured in such a manner that:

one node in the switching circuit for the emphasis circuit is connected to a source of an NMOS transistor, a drain of the NMOS transistor is connected to the power supply on the high potential side, and a gate of the NMOS transistor is connected to one terminal of a bias power supply for the emphasis circuit; and

the other node in the switching circuit for the emphasis circuit is connected to a source of a PMOS transistor, a drain of the PMOS transistor is connected to the power supply on the low potential side, and a gate of the PMOS transistor is connected to other terminal of the bias power supply for the emphasis circuit.

12. The differential drive circuit for low voltage differential signals according to claim 11, wherein the switching circuit for the emphasis circuit is the switching circuit according to claim 2.

13. An electronic apparatus comprising a differential drive circuit for low voltage differential signals according to any one of claims 1 through 12.

14. The electronic apparatus according to claim 13, wherein the electronic apparatus is constituted by a mobile terminal.